REMARKS

Claims 1, 4, 5, 9, 10, and 13-21 will be pending in the current Application upon entering this Amendment. Claims 1, 9, and 10 have been amended; claims 2, 3, 6, and 7 have been cancelled without prejudice; and dependent claim 21 has been added. Applicant submits that the amendments do not add new matter to the current Application. Applicant also submits that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Specification

With respect to the title, Applicant is amending the title to: METHOD AND APPARATUS FOR INTERFACING A PROCESSOR TO A COPROCESSOR IN WHICH THE PROCESSOR IS CAPABLE OF SELECTIVELY BROADCASTING TO THE COPROCESSOR. Applicant submits that this new title is more clearly indicative of the invention to which the claims are directed due to cancellation of non-elected claims.

Claim Rejections

Applicant respectfully submits that claim 1, 4, 5, 9, 10, and 18-21 are patentable under 35 U.S.C. 102(e) over US Patent No. 6,223,277 (hereinafter referred to as Karguth). With respect to claim 1, Applicant has amended claim 1 to further include "providing storage circuitry which stores the broadcast specifier, the broadcast specifier comprising a plurality of broadcast indicators, each broadcast indicator within the plurality of broadcast indicators corresponding to one of the plurality of registers and indicating whether or not a write to the corresponding register is to be broadcasted via the coprocessor communication bus." Claim 1 has been further clarified to indicate that the operand is provided or not provided to said coprocessor communication bus based on what the broadcast indicator corresponding to the selected one of the plurality of registers indicates. Applicant submits that at least this is not taught or suggested

by Karguth. The Examiner states that broadcast specifier is taught in Karguth by bits 15:0 of a store or load instruction which can be used to transfer data to and from registers 42. However, this field simply indicates a particular source and destination register (in registers 24 and 42) and indicates a particular location within the destination register for a particular instruction. More specifically, the Examiner, in referring to previous claim 2, indicates that the broadcast indicators is taught by bit locations 15:8 of the instruction. However, this does not teach or suggest storing a plurality of broadcast indicators where each broadcast indicator corresponds to one of a plurality of registers and indicates whether or not that corresponding register is to be broadcasted. That is, a particular register indicated within a field of a particular instance of an instruction does not provide information as to whether or not a write to each of a plurality of registers in a register file is to be provided to a coprocessor bus, as claimed in claim 1. Therefore, for at least these reasons, Applicant submits that claim 1 is patentable over Karguth.

Claims 4-5 and 21 have not been independently addressed since they depend directly or indirectly from allowable claim 1 and are therefore also allowable for at least those reasons provided with respect to claim 1.

With respect to claim 9, Applicant has amended claim 9 to further clarify that the current execution region "corresponds to a range of instruction addresses in which a current address indicated by a program counter of the processor falls." Applicant submits that at least this is not taught or suggested by Karguth. Again, the Examiner indicates that bits 15:8 of the instruction code teaches the current execution region. However, the indication of a source register in a particular instance of an instruction does not teach or even suggest a current execution region as claimed in claim 9. Furthermore, a current address indicated by a program counter of processor 25 of Karguth does not fall within a value indicated by bits 15:8. Therefore, for at least these reasons, Applicants submit that claim 9 is allowable over Karguth.

With respect to claim 10, Applicant has amended claim 10 to clarify that the plurality of broadcast indicators within the set of broadcast specifiers is stored within storage circuitry of the processor. Applicant submits that Karguth at least does not teach or suggest the set of broadcast specifiers and plurality of broadcast indicators as claimed in claim 10. As described above in reference to claim 1, the indication of a source register in bits 15:8 in a particular instance of an instruction does not teach or suggest a plurality of broadcast indicators which indicates, for each of a plurality of registers, whether or not writes to each register are to be broadcasted.

Furthermore, the Examiner indicates that the compare circuitry of claim 10 is taught by processor 25 where COPA is the broadcast enable signal. However, processor 25 does not compare bits 15:8 with any registers, and furthermore, COPA is a bus and not a signal which enables or disables an operand to be provided by element 41 (which the Examiner indicates teaches the port of claim 10). That is, COPA provides addresses from element 41 as instructed by instructions, but does not itself determine if an operand is to be provided or not. Therefore, for at least these reasons, Applicant submits that claim 10 is allowable over Karguth.

With respect to claim 18, Applicant submits that Karguth does not teach or suggest each and every element of the claim. For example, Karguth at least does not teach or suggest an execution region control unit which indicates when an address location indicated by a program counter falls within one of a set of execution regions, where each execution region indicates a range of instruction addresses. Karguth also at least does not teach or suggest indicating a current execution region when the indicated address location falls within one of the set of execution regions. Again, the Examiner indicates that an execution region is taught by bits 15:8. However, bites 15:8 do not indicate ranges of instruction addresses. The Examiner states that bits 15:8 "indicate an address range of regions within a register." However, bits 15:8 indicate a particular source address and not a range of addresses. Furthermore, claim 18 specifically states that an execution region indicates *a range of instruction addresses*, and an address range of regions within a register does not teach or suggest a range of *instruction addresses*. Also, there is nothing in Karguth which determines a particular execution region (i.e. a particular range of instruction addresses) in which an indicated address location of a program counter falls. That is, the cited sections of Karguth do not even mention use of a program counter. Therefore, for at least these reasons, Applicant submits that claim 18 is allowable over Karguth.

Claims 19 and 20 depend directly or indirectly from allowable claim 18 and are therefore also allowable for at least those reasons which apply to claim 18.

Conclusion

Although Applicant may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicant is not discussing all these statements in the current Office Action, yet reserve the right to address them at a later time if necessary.

Applicant respectfully solicits allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

Respectfully submitted,

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